L Number	Hits	Search Text	DB	Time stamp
1	6370	register with window$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:11
2	7899	register$1 with window$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:11
3	426	(register with window$3) and RISC	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:14
4	23	((register with window$3) and RISC) and (717/$.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:40
5	337	"register windows"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:42
6	54	"register windowing"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:52
7	1	"register pressuring"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:53
8	4	register with pressuring	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:54
9	6703	register$1 with pressur$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:54
10	1436	(register$1 with pressur$3).ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:55
11	218	717/159.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:56
12	121	717/153.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:56
13	220	717/158.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/20 13:56

L Number	Hits	Search Text	DB	Time stamp
1	475	712/228.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB	2004/10/20 15:01

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Terms used **register windowing** and **register types**

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1 Architectural support for reduced register saving/restoring in single-window register files
Miquel Huguet, Tomás Lang
February 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 1

Full text available: pdf(2.28 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The use of registers in a processor reduces the data and instruction memory traffic. Since this reduction is a significant factor in the improvement of the program execution time, recent VLSI processors have a large number of registers which can be used efficiently because of the advances in compiler technology. However, since registers have to be saved/restored across function calls, the corresponding register saving and restoring (RSR) memory traffic can almost eliminate the overall reduc ...

2 A simple interprocedural register allocation algorithm and its effectiveness for LISP
Peter A. Steenkiste, John L. Hennessy
January 1989 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 11 Issue 1

Full text available: pdf(2.56 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Register allocation is an important optimization in many compilers, but with per-procedure register allocation, it is often not possible to make good use of a large register set. Procedure calls limit the improvement from global register allocation, since they force variables allocated to registers to be saved and restored. This limitation is more pronounced in LISP programs due to the higher frequency of procedure calls. An interprocedural register allocation algorithm is developed by simp ...

3 The priority-based coloring approach to register allocation
Fred C. Chow, John L. Hennessy
October 1990 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 12 Issue 4

Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Global register allocation plays a major role in determining the efficacy of an optimizing compiler. Graph coloring has been used as the central paradigm for register allocation in modern compilers. A straightforward coloring approach can suffer from several shortcomings. These shortcomings are addressed in this paper by coloring the graph using a priority ordering. A natural method for dealing with the spilling emerges from this approach. The detailed algorithms for a priority-based colori ...

Published before April 2000
Terms used **register pressuring** and **register types**

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1 Optimal register assignment to loops for embedded code generation
David J. Kolson, Alexandru Nicolau, Nikil Dutt, Ken Kennedy
April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available: pdf(449.13 KB) Additional Information: full citation, abstract, references, citings, index terms, review

One of the challenging tasks in code generation for embedded systems is register assignment. When more live variables than registers exist, some variables will necessarily be accessed from data memory. Because loops are typically executed many times and are often time-critical, good register assignment in loops is exceedingly important as accessing data memory can degrade performance. The issue of finding an optimal register assignment to loops has been open for some time. In this article, ...

Keywords: code generation, embedded systems, system design

2 Improvements to graph coloring register allocation
Preston Briggs, Keith D. Cooper, Linda Torczon
May 1994 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 16 Issue 3

Full text available: pdf(2.00 MB) Additional Information: full citation, abstract, references, citings, index terms, review

We describe two improvements to Chaitin-style graph coloring register allocators. The first, optimistic coloring, uses a stronger heuristic to find a k-coloring for the interference graph. The second extends Chaitin's treatment of rematerialization to handle a larger class of values. These techniques are complementary. Optimistic coloring decreases the number of procedures that require spill code and reduces the amount of spill code when sp ...

Keywords: code generation, graph coloring, register allocation

3 Iterated register coalescing
Lal George, Andrew W. Appel
January 1996 **Proceedings of the 23rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages**

Full text available: pdf(955.09 KB) Additional Information: full citation, references, citings, index terms

4 Compiler transformations for high-performance computing